Abstract of the Disclosure

A silicon-on-insulator integrated circuit comprises a handle die, a substantially continuous and unbroken silicide layer over the handle die, and a substantially continuous and unbroken first dielectric layer overlying one side of the silicide layer. A device silicon layer having an upper surface overlies the first dielectric layer, and a second dielectric layer on the handle die underlies the opposite side of the silicide layer. [Interconnected transistors are disposed in and at the upper surface of the device silicon layer.] A silicon-on insulator integrated circuit includes a handle die and a first dielectric layer formed on the handle die. A substantially [continuous and unbroken silicide layer] is formed on the first dielectric layer; the silicide layer has a controlled resistance and provides a diffusion barrier to impurities. A substantially [continuous and unbroken second dielectric layer] is disposed between the silicide layer and a device silicon layer, and trenches extend through the device silicon layer and silicide layer and separate the device silicon layer into islands, each having an underlying continuous silicide area. [Interconnected transistors are disposed in and at an upper surface of the device silicon layer.] A bonded wafer integrated circuit comprises a handle die and [a homogeneous silicide layer bonded to the handle die. A device layer is bonded to the silicide layer, and interconnected transistors are disposed in and at a surface of device layer. The [silicide layer] (bonded zone) comprises bonding material that differs from material in the portion of the handle die adjacent the silicide layer and also differs from material in the portion of the device layer adjacent the silicide layer].